

Source: sooperkanoon.com/act/41447

Semiconductor Integrated Circuits Layout-design Act, 2000

Section 19 - Registration to Be Prima Facie Evidence of Validity

(1) In all legal proceedings relating to a layout-design registered under this Act (including application under section 30), the original registration of the layout-design and all subsequent assignments and transmissions of layout-design shall be prima facie evidence of the validity thereof.

(2) In all legal proceedings as aforesaid, a registered layout-design shall not be held to be invalid on the ground that it was not a registerable layout-design under section 7 except upon evidence of originality and that such evidence was not submitted to the Registrar before registration.
